DRAM Device Circuits and Architecture

Credit where credit is due:
Slides contain original artwork (© Jacob, Wang 2005)
Overview

![Diagram of memory system components: Processor, System Controller, Memory Controller, DRAM Module, DRAM Devices.]

- Processor
- System Controller
- Memory Controller
- DRAM Module
- DRAM Devices
Storage Cells

3T1C storage cell
1T1C storage cell (classic DRAM)
6T storage cell (classic SRAM)

DRAM: Dynamic Random Access Memory

How long does “memory storage” last?

Cell capacitance vs Leakage current
Storage Cell Structure I

plate capacitor

\[ C = \varepsilon \frac{A}{d} \]

Shrinking DRAM devices means reduced cross section (area)

above silicon in poly

below silicon surface in trench
Storage Cell Structure II

Access transistor
stacked capacitor
wordline
bitline

access transistor
n+ p well

bitline
wordline
gate
n+ p well

metal 1 bitline
poly 2
poly 3
bitline contact
poly 1 wordline

bitline
wordline
poly-silicon storage
insulating dielectric
buried n+ plate

much deeper trench
deep trench
DRAM Array I

Polycide Bitlines

8F² cell
(F = feature size. 90nm etc)

Unlayered DRAM Cell Array
DRAM Array II

- Bitlines @ $V_{\text{ref}}$
- Wordlines
- Sense amp array
- I/O gating
- $1024 \times 16$
- Row select
- Wordline
DRAM Array III (folded bitline)

2 Bitline lanes through each cell (larger cell size)
Cell size: typically 8 F²
Better noise tolerance (common mode rejection)
DRAM Array IV (Open Bitline)

- Dummy structures at array edges
- 1 Bitline lane through each cell
- Cell size: typically 6 $F^2$
- Bitline pairs come from different array segments

Challenge: How to get good noise tolerance AND small cell size?
Sense Amplifier

Wordlines

Bitline

EQ CSL

output

output

WRITE driver

WRITE driver

WRITE driver

WRITE driver

Vcc

Vcc

sensing circuit

voltage eq. circuit

SAN

SAP

EQ

CSL

WE

Differential

Control Signals
Array Precharge

Assert equalize, Array precharged to $V_{\text{ref}}$ (typically $V_{\text{cc}}/2$)

Voltage color chart:

- $0$
- $V_{\text{ref}} -$
- $V_{\text{ref}}$
- $V_{\text{ref}} +$
- $1$
Row Access I

selected row (wordline) activated

timeline

Wordlines

Bitline

Vref+

Vref

Vref

input write driver

output

input write driver

output

selected row (wordline) activated

timeline

Vcc+Vt

Vcc

(Vref) Vcc/2

Gnd

SAN

SAP

EQ

CSL

WE

tRCD

tRAS

tRP

Access

Sense

Restore

Precharge
Row Access II (sense)

SAN and SAP control signals active
lower NFet more conductive, upper PFet more conductive.
Bitline pairs slammed to opposite voltage rails, then upper
NFet and lower PFet shut off completely.

0 \quad V_{ref}^{-} \quad V_{ref} \quad V_{ref}^{+} \quad 1

Voltage color chart

()
Row Access III (Restore)

Wordline kept open, now sensing circuit drives the full voltage level "1" back into cell. If the column is selected, data is driven out to rest of the world.

Timeline

Voltage color chart
Write (over old data)

Wordline is still open, input write driver drives the full voltage level “0” into cell.

Vcc

Vcc/2

Vref

Vref –

+Vref

Gnd

Access

Sense

Restore

Write Recovery

tWR

tRP

Precharge

timeline

Voltage color chart
Decoders and Redundancy

Challenge: How to get good yield and tolerate *some* defect?
Programmable Decoders I

- Standard decoder (each row has one):
  - Functionally equivalent to NOR gate without output that can be disabled by laser (or fuse).
- Spare decoder (each spare row has one):
  - Functionally equivalent to NOR gate with inputs that can be selectively disabled.

\( \bigotimes \) (laser) programmable link.
Suppose that row 0b1010 is defective.

4 address bits select 1 of 16 rows.

blast it with laser
replace standard decoder with spare row decoder

a_3 + a_2 + a_1 + a_0
Device Control Logic

SDRAM Control Logic

FPM

Remember SAN and SAP? Something has to control sequence and timing
Mode Register

Modern DRAM devices (SDRAM, Direct RDRAM, DDRx SDRAM, etc. have programmable behaviour)
Load value from address bus with special command.
Data I/O

2N Bit prefetch in DDR SDRAM devices
4N in DDR2 SDRAM devices, and
8N in DDR3 SDRAM devices
Allows “core” to run at slower data rates while interface data rate cranks up.
Drawback - minimum burst lengths (loss of “randomness”)
SDRAM Device

Find bank 0, row 0x02F1, column 0x0EA and get an A
Package and Pincount I

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ITRS Roadmap

Package Evolution
(higher pin count, higher datarate)
(higher costs, testing etc.)
Package and Pincount II

SDRAM “Same pinout”, except for data bus
Process Technology

- Metal Interconnections: 2 layers of Al
- Inter-layer Dielectric: low K SiO₂
- 7+ layers of Cu
- layer of Tungsten

- Polysilicon: 4+ layers: cell capacitance
- Transistors: high V_t: leakage optimized
- low V_t: Drive current optimized

- trench capacitors: bulk silicon
- Substrate: BOX: Buried Oxide layer

- DRAM Optimized Process
- Logic Optimized Process